

ABSTRACT

A method and system for bootstrapping a processor from a volatile memory device connected to the processor is disclosed. The first processor is bootstrapped from flash device. The reset lines of the second processor are asserted. The boot code for
5 the second processor is loaded from the flash device into the volatile memory device.

The reset lines of the second processor are de-asserted, wherein the processor then boots from the boot code stored in the volatile memory device. The same bootstrapping method can be extended to multi-drop systems where number of secondary processor can be more than one. A switchable means for the second processor to
10 boot from volatile memory as described or from flash memory. A method also describes a mechanism to boot from synchronous volatile memory devices.